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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,693	04/30/2001	Erik R. Altman	Y0R9-2000-0844 US (8728-4	2678

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EXAMINER
HUISMAN, DAVID J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/06/2004

Frank Chau
F. CHAU & ASSOCIATES, LLP
Suite 501
1900 Hempstead Turnpike
East Meadow, NY 11554

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/845,693	ALTMAN ET AL.
	Examiner	Art Unit
	David J. Huisman	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 5/17/2004. It has been noted by the examiner that on page 2 of the amendment, a paragraph has been replaced at page 3, line 1. However, it should say page 3, line 22.

Specification

3. The disclosure is objected to because of the following informalities: On page 12, line 4, replace "301-305" with --311-315--.

Appropriate correction is required.

Claim Objections

4. Claim 14 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. More specifically, claim 14 seems to be almost identical to the added portion of claim 11.

5. Claim 19 is objected to because of the following informalities: Replace "the execution bandwidth" with --an execution bandwidth-- and replace "the fetch/issue bandwidth" with --a fetch/issue bandwidth--. Appropriate correction is required.

6. Claim 21 is objected to because of the following informalities: Replace the last occurrence of "instructions" in line 9 of the claim with --control signals--. Also, in the 4th to last line of the claim, replace "predecoded instruction" with --predecoded instructions--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 11 recites the limitation "the decoded instructions" in line 6 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soni, U.S. Patent No. 6,223,254, as applied in the previous Office Action, in view of Chan, U.S. Patent No. 5,317,745, as applied in the previous Office Action.

11. In regard to claim 1:

12. Soni teaches a method for processing a first instruction form (fig. 3, instructions stored in instruction cache 40; col. 8, lines 28-29) and a second instruction form (fig. 3, decoded instructions stored in parcel cache 52; col. 9, lines 20-23) of an instruction set in a processor comprising the steps of:

storing a plurality of instructions of the second form (decoded instructions [col. 9, lines 20-23] are stored in a parcel cache 52) proximate to a plurality of execution units (fig. 3 shows the parcel cache proximate to the execution units);

executing at least one instruction of the first instruction form in response to a first counter (Although not explicitly mentioned, it is deemed inherent to have a program counter for fetching instructions from memory which are to be subsequently executed otherwise the processor would not know from which location to fetch an instruction from); and

executing at least one instruction of the second instruction form (col. 9, lines 30-33, 11-13).

13. Soni differs from the instant invention in that while it does store a plurality of instructions of the second form in a buffer (parcel cache) proximate to the execution units, it does not store them in **a plurality of buffers** and furthermore although it must execute at least one instruction of the second form (decoded instruction) inherently in response to a certain program counter invoked by a branch instruction of the first form (fig. 4 shows that the decoded instructions of the REP LODS AL instruction are stored in the parcel cache. These decoded instructions in the parcel cache 52 are executed when the branch instruction (JNZ.CC.XXXX) of the first

instruction form in the instruction cache 40 targets the REP LODS AL instruction [col.12, lines 55-58]), but it does not specifically mention that the second instruction form is executed in response to at least one **second counter**, wherein the **second counter is invoked** by a branch instruction of the first form.

14. "Official Notice" is taken that it is well known and expected in the art that a buffer split into a plurality of smaller buffers is has the benefit of less complex indexing circuitry leading to faster lookups.

15. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the parcel cache by splitting it into a plurality of buffers.

16. One would have been motivated to do so to benefit from faster lookup times and hence faster processing.

17. However this combination still differs from the invention because it does not teach the second counter.

18. Chan teaches that by using a general program counter for the main program and an alternate program counter for a subroutine, latency in stack processing and therefore switching between program counters can be cut drastically (col. 2, lines 42-49; col. 8, lines 32-34).

19. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a second (program) counter for the instructions of the second form which are stored in the parcel cache.

20. One would have been motivated to do so because it would allow for lower latency in switching between program counters and therefore processing speed.

21. In regard to claim 5:

22. Soni discloses the method of claim 1, wherein the step of executing at least one instruction of the second instruction form further comprises the steps of:

fetching at least one instruction of the second instruction form from a buffer of the plurality of buffers (parcel (or decoded instruction) is fetched from parcel cache and sent to the reservation station [col. 9, lines 29-34]); and

sequencing the at least one instruction of the second instruction form to the execution units (Although not mentioned explicitly, col. 9, lines 11-13 disclose that the instructions are sent (sequenced) from the reservation station to the execution units).

23. In regard to claim 6:

24. Soni discloses the method of claim 1, wherein the second instruction form is a logical subset of the first instruction form (col. 9, lines 20-23 and col. 10, lines 1-2 indicate that the second instruction form is a decoded version of the first instruction form hence making it a logical subset of the first instruction form).

25. In regard to claim 7:

26. Soni discloses the method of claim 1, wherein the step of executing at least one instruction of the first instruction form further comprises the steps of:

fetching an instruction of the first form from a memory (col. 5, lines 40-49);

decoding the instruction (col. 5, lines 55-56); and

issuing the decoded instruction to at least one execution unit (col. 5, lines 55-60).

27. In regard to claim 8:

28. Soni differs from the limitations of claim 8, namely it does not posses a switch bit to signal return to fetching of the first instruction form but discloses that a return to fetching of the first instruction form is signaled by a return instruction of the second instruction form stored in a buffer of a branch unit (Although not explicitly mentioned, it is deemed inherent to the processor that a return instruction (a type of branch instruction), executed and hence stored in a buffer of a branch unit, would address an instruction to be fetched i.e. signal fetching of the first instruction form because a return instruction commonly occurs after the execution of a loop (frequently executed instructions of the second form) which would instruct the processor to fetch from a section of code that is not frequently executed i.e. first instruction form instructions. This would result in a "hit" in the memory and not in the parcel cache col. 9, lines 31-33]).

29. "Official Notice" is taken that it is well known and expected in the art to have a status bit indicating the state of a signal (e.g. a Zero bit of a status register) to simplify processing of the signal.

30. It would have been obvious to one of ordinary skill in the art at the time of the invention to add a switch bit indicating the control signal of the return instruction.

31. One would have been motivated to do so in order to simplify processing and as it is common practice in the art.

32. In regard to claim 9:

33. Soni discloses the method of claim 1, wherein a return to fetching of the first instruction form is signaled (col. 12, lines 45-46, the JUMP instruction indicates to fetch the next instruction i.e. the instruction of the first form after the REP LODS AL in the instruction cache) by a return instruction of the second instruction form stored in a buffer (fig. 4 shows the return instruction (JUMP) of the second instruction form in the parcel cache) of a branch unit.

34. Claims **2-3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Soni in view of Chan, as applied to above, and further in view of Lavi, U.S. Patent No. 6,453,407.

35. In regard to claim 2:

36. Soni differs from the instant invention because the instructions of the first form and instructions of the second form are generated by the processor (and its LRU replacement algorithm) and not generated by a compiler wherein instructions of the second form are statically loaded into the plurality of buffers.

37. Lavi has taught a system in which the compiler decodes instructions and stores them in an array for use during runtime. This prevents complex decoding of these instructions during runtime, which in turn leads to the reduction hardware decoders and required chip area. In addition, performance is improved because the time-consuming portion of the decoding would be done prior to runtime. See column 11, lines 39-59.

38. Therefore it would have been obvious to one of ordinary skill in the art to modify Soni, such that the processor hardware used to fill the parcel cache is eliminated in lieu of the compiler performing the decoding and storing of the instruction.

39. One would have motivated to do so because by using the compiler to perform the function of the hardware, hardware is reduced, performance is increased, and chip area and cost are reduced, as explained by Lavi.

40. In regard to claim 3:

41. Soni discloses that the second form of instructions are more frequently executed than the instructions of the first form (col. 2, 43-47; col. 7, lines 22-25; LRU (Least Recently Used algorithm results in the parcel cache holding instructions that are executed more frequently).

42. Claims **4** and **10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Soni in view of Chan, as applied above, and further in view of Johnson, "Superscalar Microprocessor Design," Prentice Hall, 1991 (as disclosed in the previous Office Action and herein referred to as Johnson).

43. In regard to claim 4:

44. Soni differs from the instant invention in that he does not disclose the limitations for claim 4, namely a plurality of execution queues storing the first instruction form, de-gating the plurality of execution queues and pausing fetching from memory when executing at least one instruction of the second form.

45. Johnson teaches that distributed reservation stations corresponding to separate functional units, as compared to a centralized reservation station/window design, have the benefit of less complex circuitry because you need to select among a less number of instructions to issue, no

need to for arbitration circuitry as only one instruction is issued from a distributed reservation station, and it does not need to be able to hold all instruction-types; only the type specific to its functional unit (pg. 134, lines 1-22).

46. "Official Notice" is taken that it is well known and expected that a smaller reservation station reduces complexity and minimizes lookup time.

47. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the centralized execution queue (reservation station, fig. 3) by separating it into a plurality of queues.

48. It would also have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor by providing the instructions of the second form (decoded instructions) in the parcel cache directly to the execution units (fig. 3, 60,61,71,80,90) as taught by Soni (col. 10, lines 29-31; "other pipeline stage") instead of the reservation station because this would lead to a smaller reservation station as it would not require as many entries. Inherently this would require de-gating the execution queues (reservation stations) and stopping fetching from a memory to prevent the instructions of the first type from executing.

49. One would have been motivated to make these modifications because it would lead to less complex circuitry and hence faster processing as taught by Johnson.

50. In regard to claim 10:

51. Soni in view of Chan as applied to claim 1 teaches a plurality of buffers but does not teach that each execution unit is associated with a different buffer of the plurality of buffers.

52. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to design the processor such that each execution unit is associated with one buffer by distributing the parcel cache into as many buffers as execution units and having one for each. One would have been motivated to do so because from the teachings of Johnson, circuit complexity is reduced if you have a different buffer for every execution unit because there would be no need for arbitration circuitry as only one instruction is issued from a buffer and each buffer has to be able to store only one type of decoded instruction-type.

53. Claims **11-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Soni, as applied above, in view of Johnson, as applied above.

54. In regard to claim 11:

55. Soni discloses a processor for processing a first instruction form (fig. 3, instructions stored in instruction cache 40; col. 8, lines 28-29) and a second instruction form (fig. 3, decoded instructions stored in parcel cache 52; col. 9, lines 20-23) of an instruction set comprising:

a plurality of execution units for receiving instructions (fig. 3, 60,61,71,80,90);

a branch unit (col. 8, lines 23-26, 35-38; fig. 3, BTB 42) connected to an instruction fetch unit (col. 8, lines 28-30; fig. 3, instruction streaming buffer 53) for the first instruction form and a sequencer (col. 9, lines 29-31; fig. 3, instruction streaming buffer 53) for the second instruction form;

a decode unit for decoding instructions of the first instruction form into control signals for the execution units (col. 5, lines 55-56; fig. 3, 54,55, 45-49).

56. Soni differs from the current invention because it does not disclose that the sequencer controls a plurality of gates connected between a plurality of execution queues for storing the decoded instructions of the first instruction form and the plurality of execution units.

57. Johnson teaches that distributed reservation stations corresponding to separate functional units, as compared to a centralized reservation station/window design, have the benefit of less complex circuitry because you need to select among a less number of instructions to issue, and there would be no need for arbitration circuitry because only one instruction is issued from a distributed reservation station, and it does not need to be able to hold all instruction-types; only the type specific to its functional unit (pg. 134, lines 1-22).

58. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the centralized execution queue (reservation station, fig. 3) by separating it into a plurality of queues.

59. It would also have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor by providing the instructions of the second form (decoded instructions) in the parcel cache directly to the execution units (fig. 3, 60,61,71,80,90) as taught by Soni (col. 10, lines 29-31; "other pipeline stage") instead of the reservation station because this would lead to a smaller reservation station as it would not require as many entries. This would require the sequencer (fig. 3, instruction streaming buffer 53), which is responsible for sending the instructions of the second form to be executed to disconnect the execution queues (reservation stations) from the execution units to prevent the instructions of the first type from executing. A plurality of gates connected between the execution queues and the execution units would be required for this purpose.

60. One would have been motivated to make these modifications because it would lead to less complex circuitry and hence faster processing as taught by Johnson.

61. Soni also differs from the current invention because it does not disclose the limitation of having a plurality of buffers but discloses only a single buffer (parcel cache 52), proximate to the execution units (fig. 3 shows the parcel cache proximate to the execution units), for storing predecoded instructions of the second instruction form (col. 5, lines 55-56).

62. "Official Notice" is taken that it is well known and expected in the art that a buffer split into a plurality of smaller buffers is has the benefit of less complex indexing circuitry leading to faster lookups.

63. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the parcel cache by splitting it into a plurality of buffers

64. One would have been motivated to do so to benefit from faster lookup times and hence faster processing.

65. In regard to claim 12:

66. Soni in view of Johnson has taught a processor as described in claim 11. Soni has further taught that the instructions of the first form and instructions of the second form are generated based on execution frequency, wherein instructions of the second form are executed more frequently than instructions of the first form (col. 2, 43-47; col. 7, lines 22-25; LRU (Least Recently Used algorithm results in the parcel cache holding instructions that are executed more frequently). So, overall, two types of instructions are generated: a first type (second form), which are instructions that are frequently executed and stored in the parcel cache, and a second

type (first form) which comprises those left-over instructions which are not frequently executed. This is how the two forms of instructions are defined.

67. In regard to claim 13:

68. Soni discloses the processor of claim 11, wherein the sequencer (fig. 3, instruction streaming buffer 53), engaged by the branch unit (fig. 3, BTB 42), addresses the decoded instructions of the second instruction form stored in the buffers and sequences predecoded instructions of the second instruction form to the execution unit (the instruction streaming buffer fetches instructions from the parcel cache on a "hit" and sends them to the reservation stations to be executed [col. 9, lines 29-33, 12-13]).

69. In regard to claim 14:

70. Soni differs from the instant invention in that he does not disclose the limitations for claim 14, namely a plurality of execution queues storing the decoded instructions of the first instruction form and the sequencer connected to and controlling a plurality of gates between the execution queues and execution units.

71. Johnson teaches that distributed reservation stations corresponding to separate functional units, as compared to a centralized reservation station/window design, have the benefit of less complex circuitry because you need to select among a less number of instructions to issue, and there would be no need for arbitration circuitry because only one instruction is issued from a distributed reservation station, and it does not need to be able to hold all instruction-types; only the type specific to its functional unit (pg. 134, lines 1-22).

72. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the centralized execution queue (reservation station, fig. 3) by separating it into a plurality of queues.

73. It would also have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor by providing the instructions of the second form (decoded instructions) in the parcel cache directly to the execution units (fig. 3, 60,61,71,80,90) as taught by Soni (col. 10, lines 29-31; "other pipeline stage") instead of the reservation station because this would lead to a smaller reservation station as it would not require as many entries. Inherently this would require the sequencer (fig. 3, instruction streaming buffer 53), which is responsible for sending the instructions of the second form to be executed to disconnect the execution queues (reservation stations) from the execution units to prevent the instructions of the first type from executing. A plurality of gates connected between the execution queues and the execution units would be required for this purpose.

74. One would have been motivated to make these modifications because it would lead to less complex circuitry and hence faster processing as taught by Johnson.

75. In regard to claim 15:

76. Soni as applied to claim 11 teaches a plurality of buffers but does not teach that each execution unit is connected to a corresponding buffer of the plurality of buffers.

77. However, looking at Johnson (page 134), it would have been obvious to one of ordinary skill in the art at the time of the invention to design the processor such that each execution unit is

associated with one buffer by distributing the parcel cache into as buffers as execution units and having one for each.

78. One would have been motivated to do so because, from the teachings of Johnson, circuit complexity is reduced if you have a different buffer for every execution unit as no need to for arbitration circuitry as only one instruction is issued from a buffer and each buffer has to be able to store only one type of decoded instruction-type.

79. In regard to claim 16:

80. Soni discloses the processor of claim 11, wherein the branch unit switches the processor from the first instruction form to the second instruction form in response to a branch instruction of the first instruction form (fig. 4 shows that the decoded instructions of the REP LODS AL instruction are stored in the parcel cache. These decoded instructions in the parcel cache 52 are executed when the branch instruction (JNZ.CC.XXXX) of the first instruction form in the instruction cache 40 targets the REP LODS AL instruction [col.12, lines 55-58]).

81. In regard to claim 17:

82. Soni discloses the processor of claim 11, wherein the branch unit switches the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form (fig. 4 shows the return instruction (JUMP) of the second instruction form in the parcel cache and col. 12, lines 45-46, the JUMP instruction indicates to fetch the next instruction i.e. the instruction of the first form after the REP LODS AL in the instruction cache).

83. In regard to claim 18:

84. Soni differs from the limitations of claim 18, namely it does not posses a switch bit in a buffer of the plurality of buffers to signal the sequencer to stop fetching from the buffers and enable fetching of the first instruction form from the memory but discloses that a return to fetching of the first instruction form from the memory is signaled by a return instruction of the second instruction form executed in the branch unit (Although not explicitly mentioned, it is deemed inherent to the processor that a return instruction (a type of branch instruction), executed in the branch unit, would address an instruction to be fetched i.e. signal fetching of the first instruction form because a return instruction commonly occurs after the execution of a loop (frequently executed instructions of the second form) which would instruct the processor to fetch from a section of code that is not frequently executed i.e. first instruction form instructions. This would result in a "hit" in the memory and not in the parcel cache col. 9, lines 31-33]).

85. "Official Notice" is taken that it is well known and expected in the art to have a status bit indicating the state of a signal (e.g. a Zero bit of a status register) to simplify processing of the signal.

86. It would have been obvious to one of ordinary skill in the art at the time of the invention to add a switch bit indicating the control signal of the return instruction.

87. One would have been motivated to do so in order to simplify processing and as it is common practice in the art.

88. In regard to claim 19:

89. Soni discloses the processor of claim 11, wherein the execution bandwidth of the execution units (fig. 3 shows 5 execution units 60-61,71,80 and 90) is larger than the fetch/issue bandwidth of the first form (fig. 3 shows that **one** instruction is issued to the reservation station 50 but **five** instruction can be executed in parallel by the execution units).

90. Claims **20-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Soni in view of Johnson, as applied above, and further in view of Lavi, as applied above.

91. In regard to claim 20:

92. Soni discloses the processor of claim 11, wherein the second instruction form is a logical subset of the first instruction form (col. 9, lines 20-23 and col. 10, lines 1-2 indicate that the second instruction form is a decoded version of the first instruction form hence making it a logical subset of the first instruction form).

93. Soni has not taught that the predecoded instructions of the second instruction form are statically stored in the plurality of buffers. However, Lavi has taught a system in which the compiler decodes instructions and stores them in an array for use during runtime. This prevents complex decoding of these instructions during runtime, which in turn leads to the reduction hardware decoders and required chip area. In addition, performance is improved because the time-consuming portion of the decoding would be done prior to runtime. See column 11, lines 39-59.

94. Therefore it would have been obvious to one of ordinary skill in the art to modify Soni, such that the processor hardware used to fill the parcel cache is eliminated in lieu of the compiler performing the decoding and storing of the instruction.

95. One would have motivated to do so because by using the compiler to perform the function of the hardware, hardware is reduced, performance is increased, and chip area and cost are reduced, as explained by Lavi.

96. In regard to claim 21:

97. Soni discloses a processor for processing a first instruction form (microprocessor instruction col. 8, lines 28-29) and a second instruction form (decoded instructions col. 9, lines 20-23) of an instruction set comprising:

a plurality of execution units for receiving instructions (fig. 3, 60,61,71,80,90);

a branch unit (col. 8, lines 23-26, 35-38; fig. 3, BTB 42) connected to an instruction fetch unit (col. 8, lines 28-30; fig. 3, instruction streaming buffer 53) for the first instruction form, wherein the branch unit switches the processor from the first instruction form to the second instruction form in response to a branch instruction of the first instruction form (fig. 4 shows that the decoded instructions of the REP LODS AL instruction are stored in the parcel cache. These decoded instructions in the parcel cache 52 are executed when the branch instruction (JNZ.CC.XXXX) of the first instruction form in the instruction cache 40 targets the REP LODS AL instruction [col.12, lines 55-58]) and switches the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form (fig. 4 shows the return instruction (JUMP) of the second instruction form in the parcel cache

and col. 12, lines 45-46, the JUMP instruction indicates to fetch the next instruction i.e. the instruction of the first form after the REP LODS AL in the instruction cache).

a decode unit for decoding instructions of the first instruction form into instructions for the execution units (col. 5, lines 55-56; fig. 3, 54,55, 45-49).

an issue unit adapted to sequence decoded instructions of the first instruction form (col. 5, lines 40-45, 56-60);

the sequencer (fig. 3, instruction streaming buffer 53), engaged by the branch unit (fig. 3, BTB 42), adapted to fetch the predecoded instructions and sequence the predecoded instructions of the second instruction form (the instruction streaming buffer fetches instructions from the parcel cache on a "hit" and sends them to the reservation stations to be executed [col. 9, lines 29-33, 12-13]).

98. Soni differs from the current invention because:

a) he does not disclose a plurality of buffers but discloses only a single buffer (parcel cache 52), proximate to the execution units, for storing predecoded instructions of the second instruction form (col. 5, lines 55-56). However, "Official Notice" is taken that it is well known and expected in the art that a buffer split into a plurality of smaller buffers is has the benefit of less complex indexing circuitry leading to faster lookups. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the parcel cache by splitting it into a plurality of buffers. One would have been motivated to do so to benefit from faster lookup times and hence faster processing.

b) he does not disclose statically storing the predecoded instructions of the second instruction form in a plurality of buffers. However, Lavi has taught a system in which the

compiler decodes instructions and stores them in an array for use during runtime. This prevents complex decoding of these instructions during runtime, which in turn leads to the reduction hardware decoders and required chip area. In addition, performance is improved because the time-consuming portion of the decoding would be done prior to runtime. See column 11, lines 39-59. Therefore it would have been obvious to one of ordinary skill in the art to modify Soni, such that the processor hardware used to fill the parcel cache is eliminated in lieu of the compiler performing the decoding and storing of the instruction (statically). One would have motivated to do so because by using the compiler to perform the function of the hardware, hardware is reduced, performance is increased, and chip area and cost are reduced, as explained by Lavi.

c) he does not disclose a plurality of execution queues storing the decoded instructions of the first instruction form and the sequencer connected to and controlling a plurality of gates between the execution queues and execution units. However, Johnson teaches that distributed reservation stations corresponding to separate functional units, as compared to a centralized reservation station/window design, have the benefit of less complex circuitry because you need to select among a less number of instructions to issue, no need to for arbitration circuitry as only one instruction is issued from a distributed reservation station, and it does not need to be able to hold all instruction-types; only the type specific to its functional unit (pg. 134, lines 1-22). Consequently, it would have also been obvious to one of ordinary skill in the art at the time of the invention to modify the centralized execution queue (reservation station, fig. 3) by separating it into a plurality of queues. It would also have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor by providing the instructions of the second form (decoded instructions) in the parcel cache directly to the execution units (fig. 3,

60,61,71,80,90) as taught by Soni (col. 10, lines 29-31; "other pipeline stage") instead of the reservation station because this would lead to a smaller reservation station as it would not require as many entries. This would require the sequencer (fig. 3, instruction streaming buffer 53), which is responsible for sending the instructions of the second form to be executed to disconnect the execution queues (reservation stations) from the execution units to prevent the instructions of the first type from executing. A plurality of gates connected between the execution queues and the execution units would be required for this purpose. One would have been motivated to make these modifications because it would lead to less complex circuitry and hence faster processing as taught by Johnson.

Response to Arguments

99. Applicant's arguments filed on May 17, 2004, have been fully considered but they are not persuasive.

100. Applicant argues the novelty/rejection of claim 1 on pages 13-14 of the remarks, in substance that:

"Chan teaches that program counters correspond to interrupt devices, and that the program counters are invoked by a control logic receiving interrupt signals...Nowhere does Chan teach or suggest that the alternate program counters are invoked by a branch instruction. The flag set of Chan is not an instruction, much less a branch instruction. Therefore, Chan fails to sure the deficiencies of Soni."

"...with respect to claim 1, the Examiner has taken Official Notice that it is well known and expected in the art that a buffer split into a plurality of smaller buffers has the benefit of less complex indexing circuitry leading to faster lookups. Applicants respectfully traverse the finding of Official Notice. Merely splitting a single buffer into a number of smaller buffers is not believed to reduce the total size of the buffer needed to be searched for contents. Thus, the time needed to perform a lookup in a single buffer or a plurality of buffers having a total size similar to the single buffer would be substantially the same if not more considering the time needed for switching between the plurality of buffers. Therefore, using multiple buffers would not be an obvious alternative to a single buffer. If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. Such an affidavit is respectfully requested."

101. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, Chan has explicitly stated in column 8, lines 32-34, that multiple program counters (PCs) may be used for **regular** subroutine calls. As is known in the art, a subroutine is called by a branch instruction. If a second PC is used for a particular subroutine, then the use of this PC will be invoked when the branch instruction (which branches to the associated subroutine) is encountered.

b) Regarding the second argument, the examiner did not rely on personal knowledge in taking Official Notice. Consequently, an affidavit or declaration to show support of the item in question is not required. See MPEP §2144.03[R-1], section C. Instead, a any reference may be used to show support. The examiner would like to bring to applicant's attention Burrer et al., U.S. Patent No. 5,172,379 (herein referred to as Burrer). Burrer has taught in column 5, lines 34-43, the general idea of splitting a memory (i.e., buffer) into multiple banks in order to "reduce the complexity of the memory control logic" and also to perform parallel lookups, which as is known in the art, results in faster lookups (since each buffer can be accessed at the same time, thereby looking up multiple locations at once as opposed to a single location when using a single buffer). Consequently, the examiner asserts that the use of Official Notice is supported, and thereby maintains its use in the rejection of claim 1. Finally, as a side note, as shown in Nerwin v. Erlichman 168 USPQ 177 (1969), to make separable is generally not given patentable weight or would have been an obvious improvement for at least the reason stated above.

102. Applicant argues the novelty/rejection of claims 8-9 on pages 14-15 of the remarks, in substance that:

"Soni does not teach or suggest "a buffer of a branch unit" as claimed in claims 8 and 9. Soni teaches that a parcel cache is coupled to the fetch/parse/decide/issue unit 43, and sends parcels to a reservation station. Nowhere does Soni teach or suggest that a branch unit has a buffer."

103. These arguments are not found persuasive for the following reasons:

a) The examiner asserts that "a buffer of a branch unit" is nothing more than a name as currently claimed. As can be seen in Fig.3 and Fig.4, Soni's system has the ability to execute branch instructions (see the jump execution unit JEU in Fig.3, for instance). Therefore, Soni's system may be interpreted as a branch unit. Moreover, because Soni's system is a branch unit, and Soni's system has a buffer (parcel cache), Soni has taught a "buffer of a branch unit." Likewise, Soni can be viewed as having a branch unit (Fig.3, component 90), and as shown in Fig.4, the buffer (parcel cache) holds a branch instruction (jump at address AAAF). Clearly, the jump instruction will be executed by the branch unit and therefore, the buffer will supply the branch unit. Therefore, the parcel cache is a "buffer of a branch unit." The BTB may also be considered a branch unit with which the buffer is associated.

104. Applicant's arguments, with respect to the rejection(s)of claim(s) 2-3 under Soni in view of Chan and further in view of Ball have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Soni in view of Chan and further in view of Lavi.

105. Applicant argues the novelty/rejection of claim 11 on pages 17-18 of the remarks, in substance that:

"Soni does not teach or suggest a gate between the reservation station and the execution units. Therefore, Soni does not teach or suggest a sequencer for controlling a plurality of gates connected

between a plurality of execution queues and the plurality of execution units, essentially as claimed in claim 11."

106. These arguments are not found persuasive for the following reasons:

a) Applicant may be correct in saying that Soni does not teach such gates. However, The test of obviousness is:

> "whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," In re Gorman, 933 F.2d at 986, 18 USPQ2d at 1888.
>
> Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination." In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988).
>
> "Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." In re Wood, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).
>
> "In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found in a specific reference."
>
> Entire quote from In re Oetiker, 24 USPQ2d 1443 (CAFC 1992).

Accordingly, Soni is not required to disclose or specifically suggest particular elements. Instead the measure is what the teachings of Soni would suggest to one of ordinary skill in the art, not what Soni specifically suggests. More specifically, the examiner pointed out in the rejection of claim 11, that Soni has taught that the instructions in the parcel cache may be provided to another

stage, i.e., the execution stage. If this were the case, then instructions may either arrive for execution from either the reservation station(s) or directly from the parcel cache. Clearly, it would have been obvious to implement some mechanism (gates) which allow for selection of an instruction from either the reservation station of the parcel cache. The examiner feels that reasoning and motivation has been established in the previous Office Action, and consequently, this rejection is maintained.

107. Applicant's arguments, with respect to the rejection(s)of claim(s) 20 under Soni in view of Johnson have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Soni in view of Johnson and further in view of Lavi.

108. The examiner's response to arguments for claim 21 are the same as the response to arguments for claims 1, 2, and 11 above.

Conclusion

109. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
June 29, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100